晁元國際半導體股份有限公司

MaxPower SiC Semiconductor Co., Ltd.

M2D-1200-0080

Silicon Carbide MOSFET Bare Die

N-channel Enhancement Mode

Features

- High Blocking Voltage with Low On-Resistance
- High Speed Switching with Low Capacitances
- Easy to Parallel and Simple to Drive
- Avalanche Ruggedness
- Halogen Free, RoHS Compliant

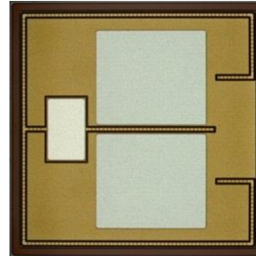
Benefits

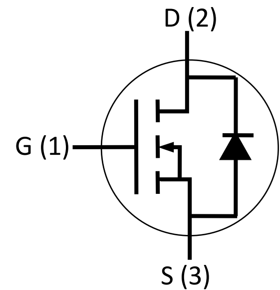
- Higher System Efficiency
- Reduced Cooling Requirements
- Increased Power Density
- Increased System Switching Frequency

Applications

- Solar Inverters
- Switch Mode Power Supplies
- High Voltage DC/DC Converters
- Battery Chargers
- Motor Drives
- Pulsed Power applications

Package





Part Number	Die Size
M2D-1200-0080	3.3mm*3.3mm

Electrical Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	1200			V	V_{GS}=0V, I_D=100μA	
$V_{GS(th)}$	Gate Threshold Voltage	2.0	2.4	4.0	V	V_{GS}= V_{DS}, I_{DS}=5mA, T_C=25°C	Fig. 6
			1.73			V_{GS}= V_{DS}, I_{DS}=5mA, T_C=150°C	
I_{DSS}	Zero Gate Voltage Drain Current		1	100	μA	V_{DS}= 1200V, V_{GS}=0V	
I_{GSS}	Gate-Source Leakage Current		20	200	nA	V_{GS}=20V, V_{DS}= 0V	
$R_{DS(on)}$	Drain-Source on-state Resistance		80	98	mΩ	V_{GS}=20V, I_D=20A, T_C=25°C	Fig. 4
			120			V_{GS}=20V, I_D=20A, T_C=150°C	
g_{fs}	Transconductance		7.0		S	V_{GS} = 20 V, I_D = 20A, T_J = 25 °C	Fig. 5
			6.6			V_{GS} = 20 V, I_D = 20A, T_J = 150 °C	
Ciss	Input Capacitance		2016		pF	V_{GS}=0V, V_{DS}=1000 V, f=1MHz V_{AC}=25 mV	Fig. 8
Coss	Output Capacitance		17.9				
Crss	Reverse Transfer		72.6				

	Capacitance						
E_{ON}	Turn-On Switching Energy		180		μJ	V_{DS}=800V, V_{GS}=-5/20V, I_D= 20A, $R_{G(ext)}$ = 5Ω, L= 142 μH	

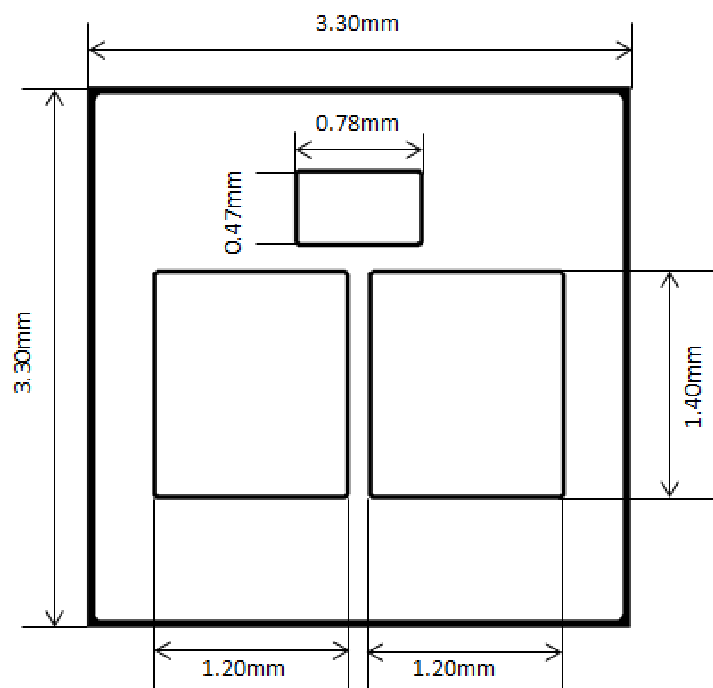
E_{OFF}	Turn-Off Switching Energy		70				
$t_{d(on)}$	Turn-On Delay Time		23		ns	V_{DD}=800V, V_{GS}=-5/20 V I_D = 20A, $R_{G(ext)}$ = 5 Ω , R_L=40Ω , Timing relative to V_{DS}	
t_r	Rise Time		60				
$t_{d(off)}$	Turn-Off Delay Time		17				
t_f	Fall Time		12				
$R_{G(int)}$	Internal Gate Resistance		2.8		Ω	f=1 MHz, V_{AC}=25mV	
Q_{gs}	Gate to Source Charge		23		nC	V_{DD}=800V, V_{GS}=-5/20 V I_D = 20A	Fig. 9
Q_{gd}	Gate to Drain Charge		26				
Q_g	Total Gate Charge		85				

Reverse Diode Characteristics

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
V_{SD}	Diode Forward Voltage	3.5		V	V_{GS} = -5V, I_{SD} = 10 A, T_J = 25 °C	Fig. 7
		3.3		V	V_{GS} =- 5V, I_{SD} = 10 A, T_J = 150 °C	
I_S	Continuous Diode Forward Current		15	A	T_C = 25°C	

Mechanical Parameters

Parameter	Typ.	Unit
Die Size	3.30*3.30	mm
Source Pad Size	1.40*1.20	mm
Gate Pad Size	0.78*0.47	mm
Die Thickness	180±30	µm
Wafer Size	150	mm
Top Side Source Metalization (Al)	4	µm
Top Side Gate Metalization (Al)	4	µm
Cathode Metalization (Ni/Ag)	1.5	µm


3.30mm
0.78mm
0.47mm
3.30mm
1.40mm
1.20mm
1.20mm